**Department of Computer Engineering**

BLG 242E  
Digital Circuits Laboratory Experiment Report

Experiment : 8 Arithmetic Logic Unit

Experiment Date : 29.04.2016

Group Number : 11

Group Members :

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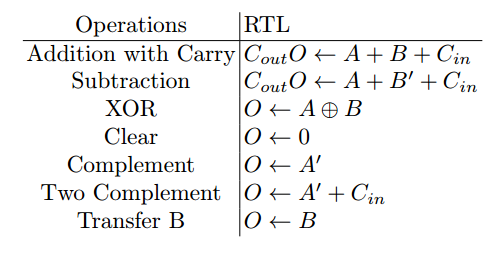
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# Introduction

Br Main objective of this experiment is to emphasize the use of sequential circuits (rather than combinational) in the realization of arithmetical and logical operations. In this manner, a serial arithmetic logical unit (sALU) is going to be designed and implemented.

# Requirements

## Part 1



In this table, O is the output bit, A and B are input bits, Cout is carry output and Cin is carry input. These are the operations that our ALU execute.

We implemented this circuit with:

- 7404 - Hex Inverters

- 7408 - Quadruple 2-input Positive-AND Gates

- 7432 - Quadruple 2-input Positive-OR Gates

- 7483 - 4-Bit Binary Full Adder with Fast Carry

- 7486 - Quad 2-Input Exclusive Or Gate

- 74151 - 8-Input Multiplexer

## Part 2

- 7404 - Hex Inverters

- 7408 - Quadruple 2-input Positive-AND Gates

- 7432 - Quadruple 2-input Positive-OR Gates

- 7483 - 4-Bit Binary Full Adder with Fast Carry

- 7486 - Quad 2-Input Exclusive Or Gate

- 74151 - 8-Input Multiplexer

- 74174 - Hex D-Type Flip-Flop with Reset

# Conclusion

Comment on any difficulties you have faced, what you have learned etc.